



SWITCHING DEVICE

This invention relates to a switching device comprising two transistors, that is, a first bipolar transistor and a second field effect or bipolar transistor.

In the following description and in the drawings, identical reference numerals are used in relation to identical or corresponding components.

A prior art arrangement and problems associated with it will now be described with reference to Fig. 2 in which is shown one embodiment of a circuit comprising two transistors in a so-called cascade arrangement.

Referring to Fig. 2, a main bipolar transistor Q1 (hereinafter referred to as a BPT), a field effect transistor Q2 (hereinafter referred to as an FET) and a zener diode ZD1 are interconnected as shown.

The collector G1 and the emitter E1 of the BPT Q1, and the drain D and the source S of the FET Q2 are connected in series at the emitter E and the drain D to enable current supplied to a load (not shown) to be switched ON-OFF (for the sake of convenience, this current is referred to herein as the collector current). Further, the transistors Q1 and Q2 are collectively referred to as a composite transistor for the sake of the convenience. The zener diode ZD1 is connected between the base B1 of the BPT Q1 and the source S of the FET Q2 in such a way that the side of the base B1 comprises the cathode side of the diode.

An ON-OFF signal voltage  $e_G$ , determining the ON-OFF state of the collector current  $I_C$ , is applied by way of a driving circuit (not shown) between the gate G and the source S of the FET Q2, while a base current  $I_{B1}$  is supplied to the base B1 via a base power source EB connected between the base B1 of the BPT Q1 and the source S of the FET Q2 when the latter is turned ON.

The circuit is arranged to provide a composite switching element at high speed and high voltage endurance by the combination of high speed and low voltage endurance characteristics of the FET Q2 and low speed and high endurance bipolar characteristics of the transistor Q1 taking notice of the fact that the switching speed of an FET is generally greater than that of a bipolar transistor.

Referring first to the case of turning the composite transistor Q1 and Q2 ON, since the FET Q2 is connected to the emitter E1 of the BPT Q1 to enable the base current  $I_{B1}$  to be turned ON and OFF in this circuit, and the base voltage  $e_B$  applied to the base B1 of the BPT Q1 can be made relatively high, when the ON-OFF signal voltage  $e_G$  is applied to the FET Q2 to turn the transistor Q2 ON, the voltage VDS between the drain D and the source S falls rapidly thereby abruptly raising the base current  $I_{B1}$  to rapidly turn BPT Q1 ON and, accordingly, both transistors Q1, Q2 are switched ON. In this case, the zener diode ZD1 is in the OFF state (non-conduction).

When turning OFF the composite transistor Q1 and Q2, an ON-OFF signal voltage  $e_G$  is applied to the FET Q2 to turn OFF the transistor Q2. The voltage VDS between the drain D and the source S of the FET Q2 abruptly increases to block the collector current  $I_c$ . At this instant, the collector current  $I_c$  flowing through the base and the emitter of the BPT Q1 is transferred to the zener diode ZD1. In this way, since carriers accumulated at the base of the BPT Q1 are rapidly discharged, the transistor Q1 and, accordingly, the composite transistor Q1 and Q2, is rapidly turned OFF to interrupt the collector current  $I_c$ .

In this case, the zener diode ZD1 is used in the transferring path as described above, so as to maintain the voltage VDS between the drain and the source of the FET Q2 to lower than a limit voltage capable of turning off (switching inhibition voltage BVDS) upon turning OFF the FET Q2, that is, upon transfer of the collector current  $I_c$ , while hindering wasteful shunting, via the zener diode, of the base current  $I_{B1}$  supplied from the base power supply EB to the connection to the base B1 of the BPT Q1, in the case where the composite transistor Q1 and Q2 is turned ON, so that it effectively forms the base current  $I_B$ .

In an actual device of this type, when the FET Q2 is turned OFF, stray inductance L1 of the wiring between the emitter E1 of the BPT Q1 and the drain D of the FET Q2 sometimes generates a transitional excessive voltage (spike voltage) in trying to maintain the previous current (indicated in broken line in Fig. 2), resulting in breakdown of the FET Q2.

In this case, the provision of means for delaying the FET Q2 to turn OFF lowers the spike voltage and breakdown of the FET Q2 can be prevented. However, on the other hand, the total switching time of the composite transistor Q1, Q2 becomes large and thereby the object of adopting this circuit for use in high frequency circuits cannot be attained.

It is an object of the present invention to provide a switching device which ameliorates said problems and makes it possible to adopt said composite transistor arrangement for use in high frequency switching circuits while effectively utilising said stray inductance L1.

According to this invention there is provided a switching device comprising a first bipolar transistor having its collector-emitter main conductive path connected in series with the main conductive path of a second transistor having a control electrode for receiving an ON-OFF control signal voltage for switching ON and OFF the second transistor so as to open and close the series-connected main conductive paths for controlling the supply of a load current, connections being provided for supplying base current to the first transistor, a third transistor having its main conductive path connected across said base current supply connections and a zener diode connected between the control electrode of the third transistor and a point between the main conductive paths of the first and second transistors such that said zener diode supplies current to the base of the third transistor to switch the latter to cause the first transistor to be switched OFF in a controlled manner, only when the voltage at said point causes the voltage across the zener diode to exceed its threshold voltage.

Embodiments of this invention will now be described, by way of example, with reference to the accompanying drawings in which:-

Figs. 1(A) and 1(B) are respective circuit diagrams of different forms of switching device embodying this invention; and

Fig. 2 is a circuit diagram of a known form of switching device embodying this invention.

In Fig. 1(A) there is shown a modified form of the switching device shown in Fig. 2 in which, instead of the zener diode ZD1, the collector C3 and emitter E3 of an auxiliary transistor Q3 are connected so as to provide a shunt circuit for the base current  $I_{B1}$  of the BPT Q1 and moreover a zener diode ZD3 is connected between a point immediately adjacent to the drain D of the FET Q2 (i.e. at a point where the stray inductance between such point and the drain D can be disregarded) and the base B3 of said auxiliary transistor Q3. In addition, the zener (threshold) voltage of the zener diode ZD3 is set lower than the maximum drain source voltage (the switching rejection voltage BVDS) of the FET Q2.

In this circuit, when the FET Q2 turns OFF, a base current  $I_{B3}$  is supplied to the base B of the auxiliary transistor Q3 through the zener diode ZD3 with a voltage induced by the stray inductance L1 so that the transistor Q3 turns ON, shunting the base current  $I_{B1}$  by providing a short-circuit between the base B of the BPT Q1 and the source S of the FET Q2 and turning OFF transistor Q1 in a controlled manner by discharging carriers accumulated at the base of the BPT Q1. Moreover, in this case, a voltage between the drain D and source S of the FET Q2 is limited by the zener (threshold) voltage of the zener diode ZD3 and thereby prevents breakdown of the FET Q2. Thus, the composite transistor Q1, Q2 can be turned OFF quickly without resulting in breakdown of the FET Q2.

In Fig. 1(B) there is shown a modified form of the device shown in Fig. 1(A) where a voltage induced by stray inductance L2 of the external line of the collector connection for collector C1 is absorbed when the BPT Q1 turns OFF and it is used for causing transistor Q1 to turn ON. In this circuit, a zener diode ZD4 is connected between a point immediately adjacent the collector C1 of the BPT Q1 (at a point where the inductance between this point and said collector C1 can be disregarded) and the base B3 of the auxiliary transistor Q3. The zener (threshold) voltage of this zener

diode ZD4 is set lower than the maximum collector-to-source voltage which can be allowed for the composite transistor Q1 and Q2.

In this circuit, when the BPT Q1 turns OFF, a base current  $I_{B31}$  is additionally supplied to the base B3 of auxiliary transistor Q3 through the zener diode ZD4 with a voltage induced by the inductance L2 and thereby said transistor Q3 is triggered to become ON and the BPT Q1, and hence the composite transistor Q1, Q2 are quickly turned OFF in a controlled manner. Moreover, since the collector-emitter voltage of the BPT Q1 is kept at a value lower than the allowable value by the appropriate selection of the zener diode ZD4 breakdown of the BPT Q1 can be prevented.

In the embodiments shown in Figs. 1(A) and 1(B), the FET Q2 may be a low voltage resistance bipolar transistor and the auxiliary transistor Q3 may be an FET, and modes of operation similar to the embodiments described above can be realised.

However, where the auxiliary transistor Q3 is an FET, the base currents  $I_{B3}$ ,  $I_{B31}$  are mostly shunted via a resistor R2 provided in parallel to the path between the base B3 and emitter E3 of the auxiliary transistor Q3.

The embodiments shown in Figs. 1(A) and 1(B) each provide the advantages that:-

1. When the switching device is turned OFF, a spike voltage generated by the stray inductance of the main circuit wiring between the first and second transistors reaches the base (gate) of a third transistor through the zener diode provided, and thereby the drain-to-source (collector-to-emitter) voltage of the second transistor is limited to almost the zener (threshold) voltage of said zener diode, avoiding breakdown of the second transistor.
2. The stray inductance can be effectively utilised for switching OFF the composite transistor.
3. The switching device can be adopted for use in high frequency circuits because the turn-OFF time of the second transistor and therefore the switching time of the composite transistor is not significantly delayed.

Thus the embodiments shown in Figs. 1(A) and 1(B) and described above provide a switching device comprising a first bipolar transistor Q1 having its collector-emitter main conductive path C1E1 connected in series with the main conductive path DS of a second transistor Q2 having a control electrode G for receiving an ON-OFF control signal voltage  $e_G$  for switching ON and OFF the second transistor Q2 so as to open and close the series-connected main conductive paths C1E1, DS for controlling the supply of a load current  $I_c$ , connections being provided for supplying base current  $I_{B1}$  to the first transistor Q1, a third transistor Q3 having its main conductive path C3E3 connected across said base current supply connections and a zener diode ZD3 connected between the control electrode of the third transistor Q3 and a point between the main conductive paths of the first and second transistors Q1, Q2 such that said zener diode ZD3 supplies current to the base of the third transistor Q3 to switch the latter to cause the first transistor to be switched OFF in a controlled manner, only when the voltage at said point causes the voltage across the zener diode ZD3 to exceed its threshold voltage.

CLAIMS:

1. A switching device comprising a first bipolar transistor having its collector-emitter main conductive path connected in series with the main conductive path of a second transistor having a control electrode for receiving an ON-OFF control signal voltage for switching ON and OFF the second transistor so as to open and close the series-connected main conductive paths for controlling the supply of a load current, connections being provided for supplying base current to the first transistor, a third transistor having its main conductive path connected across said base current supply connections and a zener diode connected between the control electrode of the third transistor and a point between the main conductive paths of the first and second transistors such that said zener diode supplies current to the base of the third transistor to switch the latter to cause the first transistor to be switched OFF in a controlled manner, only when the voltage at said point causes the voltage across the zener diode to exceed its threshold voltage.
2. A semiconductor device in which the emitter of a first transistor is connected with a drain (collector) of a second transistor, and an auxiliary DC power source is connected between the base of the first transistor and the source (emitter) of the second transistor to supply a base current to the first transistor, an ON-OFF signal voltage is applied between the gate (base) and the source (emitter) of the second transistor and an externally supplied load current is turned ON and OFF by way of a series circuit of the collector-emitter of the first transistor and the drain-source (collector-emitter) of the second transistor, wherein the collector (drain) of a third transistor is connected to the base of the first transistor, while the emitter (source) of the third transistor is connected to the source (emitter) of the second transistor respectively, and a zener diode is connected between the drain (collector) of the second transistor and the base (gate) of the third transistor with a polarity such as to allow a base current to flow to the third transistor only when the voltage at the drain (collector) of the second transistor exceeds the threshold voltage of the zener diode.

3. A switching device according to claim 1, wherein said second and/or third transistor is a field effect transistor whose drain-source path provides said main conductive path.
4. A switching device according to claim 1, wherein said second and/or third transistor is a bipolar transistor whose collector-emitter path provides said main conductive path.
5. A switching device according to claim 1, wherein said second transistor is a field effect transistor and said third transistor is a bipolar transistor.
6. A switching device according to any one of the preceding claims, wherein the point between the main conductive paths of the first and second transistors to which the zener diode is connected is made immediately adjacent the second transistor to minimise stray inductance between said point and the main conductive path of said second transistor.
7. A switching device according to any one of the preceding claims, wherein a further zener diode is connected between the control electrode of the third transistor and the side of the main conductive path of the first transistor remote from the second transistor.
8. A switching device according to claim 7, wherein said further zener diode is connected to the side of the main conductive path of the first transistor at a position immediately adjacent the latter to minimise stray inductance between said position and the first transistor.

Fig. 1(A) 1/1

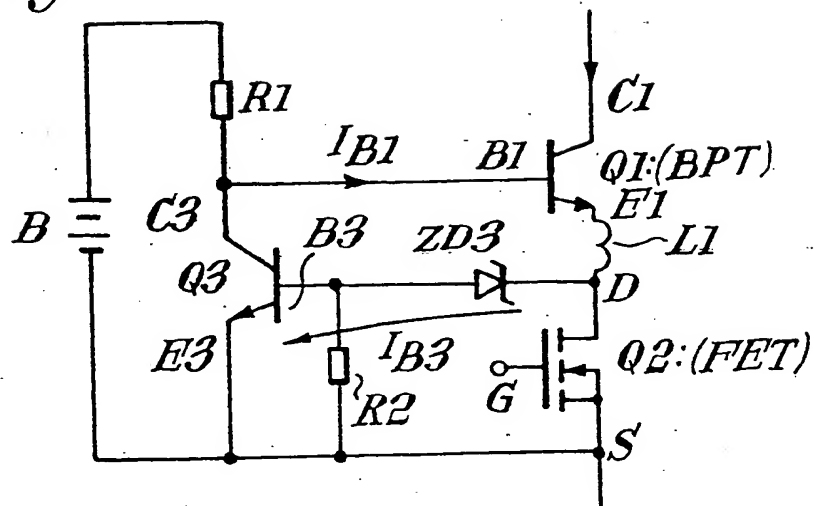


Fig. 1(B)

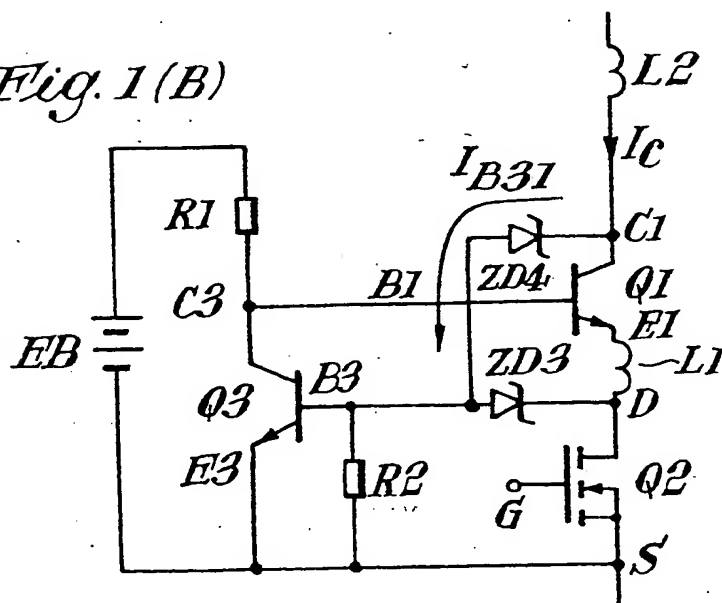
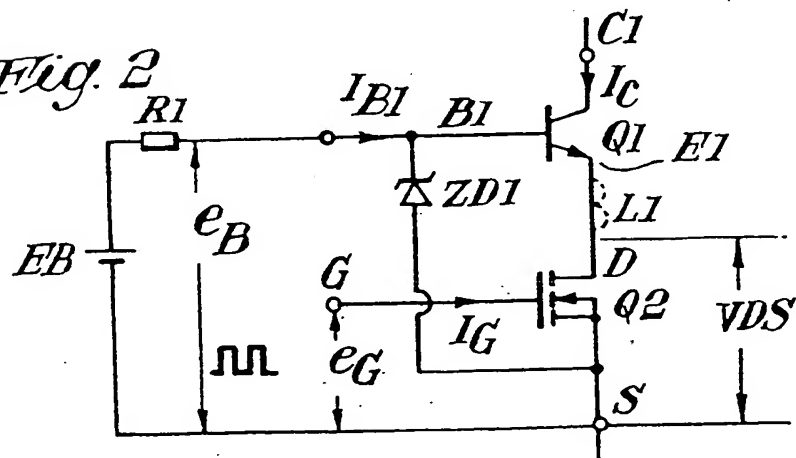


Fig. 2





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# RAPPORT DE RECHERCHE EUROPEENNE

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Numéro de la demande

EP 86 30 4599

DOCUMENTS CONSIDERES COMME PERTINENTS			
Catégorie	Citation du document avec indication, en cas de besoin, des parties pertinentes	Revendication concernée	CLASSEMENT DE LA DEMANDE (Int. Cl. 4)
A	DE-A-3 338 627 (LICENTIA PATENT-VERWALTUNGS-GMBH) * figure 1; elements 2, 3, 14; abstract; claim 1; page 3, line 15 - page 4, line 18; page 5, line 19 - page 7, line 7 *	1-3	H 03 K 17/56 H 03 K 17/04 H 03 K 17/08
A	GB-A-2 053 606 (GOULD ADVANCE LTD.) * figure 3, elements 32, 33, 41; abstract; page 2, lines 63-64 *	1-4	
A	EP-A-0 108 283 (SIEMENS AG) * figures 1, 2; abstract *	1,2	
P,A	US-A-4 547 686 (D.Y. CHEN) * figure 1; abstract *	1,2	
A	ELECTRONIQUE APPLICATIONS, no. 31, pages 35-44, August-September 1983, pages 35-44, Evry, France; "Darlington, Bipmos, Cascode: caractéristiques et critères d'emploi"	1,2	H 03 K 17/04 H 03 K 17/08 H 03 K 17/10 H 03 K 17/56 H 03 K 17/60
A	PATENT ABSTRACTS OF JAPAN, vol. 7, no. 111 (E-175)[1256], 14th May 1983; & JP - A - 58 33322(TOKYO SHIBAURA DENKI K.K.) 26-02-1983		
Le présent rapport de recherche a été établi pour toutes les revendications			
Lieu de la recherche BERLIN		Date d'achèvement de la recherche 22-08-1986	Examineur ARENDT M
<b>CATEGORIE DES DOCUMENTS CITES</b> X : particulièrement pertinent à lui seul Y : particulièrement pertinent en combinaison avec un autre document de la même catégorie A : arrière-plan technologique O : divulgation non-écrite P : document intercalaire T : théorie ou principe à la base de l'invention E : document de brevet antérieur, mais publié à la date de dépôt ou après cette date D : cité dans la demande L : cité pour d'autres raisons & : membre de la même famille, document correspondant			

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Catégorie	Citation du document avec indication, en cas de besoin, des parties pertinentes	Revendication concernée	
A	US-A-4 449 063 (H. OHMACHI et al.) * figure 9; abstract *		
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-18, no. 6, pages 773-777, December 1983; C.-Y. WU: "A new internal overvoltage protection structure for the bipolar power transistor" * figure 1 *		
Le présent rapport de recherche a été établi pour toutes les revendications			DOMAINES TECHNIQUES RECHERCHES (Int. C. 4)
Lieu de la recherche BERLIN		Date d'achèvement de la recherche 22-08-1986	Examineur ARENDE M
CATEGORIE DES DOCUMENTS CITES			T : théorie ou principe à la base de l'invention E : document de brevet antérieur, mais publié à la date de dépôt ou après cette date D : cité dans la demande L : cité pour d'autres raisons & : membre de la même famille, document correspondant
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